What is claimed is:

1. A method of detecting a peak from delay profile data received through a multi-path in a CDMA receiver, comprising the steps of:

dividing the delay profile data into a plurality of data blocks;

searching a maximum value of the delay profile data at every data block; and

keeping each maximum value at every data block to detect the peak from the maximum values searched from the respective data blocks.

2. A method as claimed in claim 1, further comprising the step of:

subsequently detecting a following peak after the peak is previously detected as a previous peak.

3. A method as claimed in claim 2, wherein the subsequently detecting step comprises the steps of:

masking a neighboring time region of the delay profile data adjacent to the previous peak to obtain renewed delay profile data;

determining, from the renewed delay profile data, a specific one of the data blocks that includes the previous peak; and

re-executing the searching step only about the specific data block to detect the following peak.

4. A method as claimed in claim 3, wherein the subsequently detecting step further comprises the steps of:

judging, before the re-executing step, whether or not the previous peak is located on a right-hand side of a center of the specific data block to produce a result of judgement; and

re-executing the searching step also about either of a right-hand side data block and a left-hand side data block adjacent to the specific data block with reference to the result of judgement, along with the specific data block.

5. A method as claimed in claim 4, wherein each of the searching step and the subsequently detection step comprises the steps of:

comparing each of the delay profile data and the renewed delay profile data with a predetermined reference correlation level; and

stopping each of the searching and the subsequently detecting steps at a time instant at which a peak lower than the predetermined reference correlation level is detected.

6. A multi-path detection circuit for use in a CDMA receiver to measure a delay profile from a multi-path and to detect timing of the multi-path, comprising:

means for dividing delay profile data representative of the delay profile into a plurality of data blocks;

a delay profile memory for storing the respective data blocks;

searching means for searching a maximum value at every one of the data blocks in connection with the delay profile data to determine a peak at every data block as a result of the search; and

generating means for generating the timing of the multi-path with reference to the peak.

7. A multi-path detection circuit as claimed in claim 6, further comprising:

means for renewing the delay profile data into renewed delay profile data by masking a neighboring time region of the delay profile data adjacent to the peak detected so as to detect a next following peak in the renewed delay profile data after the peak;

means for selecting a specific one of the data blocks that includes the peak previously detected; and

control means for making the search means search a following maximum value again only about the specific block of the renewed delay profile data.

8. A multi-path detection circuit as claimed in claim 7, wherein the control means comprises:

means for judging whether or not the previously detected peak is located on a right-hand side of a center of the specific data block, to produce a result of judgment; and

means for making the searching means re-execute the search in connection with either one of the data blocks adjacent to the specific data block on its right-hand side or left-hand side with reference to the result of judgment.

9. A multi-path detection circuit as claimed in claim 8, wherein the control means carries out a control operation such that each peak detected is compared with a predetermined reference correlation level to detect a low peak lower than the predetermined reference correlation level and the search is stopped when the low peak is detected.

10. A multi-path detection circuit comprising:

a matched filter for measuring a delay profile data of a multi-path by calculating a correlation value between a spread code and a reception signal;

a first memory selector for dividing the measured delay profile data into a plurality of data blocks;

a delay profile memory which has a plurality of memory blocks for storing the respective data blocks;

a second memory selector for selecting each of the data blocks stored in the delay profile memory;

a first maximum value searching portion for searching a block maximum value and a block maximum position at every data block selected by the second memory selector to successively produce a first result of the search;

a peak preservation portion for successively preserving the first result of the search;

a second maximum value searching portion for searching a further maximum value among the first results of the search that are preserved in the peak preservation portion and that are detected from the respective data blocks, to produce a second result of the search; and

a path timing generator for generating path timing with reference to the second result of the search.

11. A multi-path detection circuit as claimed in claim 10, further comprising:

a detected peak masking portion for masking data at a peak position and its adjacent region of the delay profile data stored in the delay profile memory by clearing the above-mentioned data from the delay profile memory.

12. A multi-path detection circuit as claimed in claim 11, further comprising:

a controller for controlling the first maximum value searching portion so that the first maximum value searching portion executes, on detecting a first peak as a previous peak, a maximum value searching operation in connection with a whole of the data blocks stored in the delay profile memory while the first maximum value searching portion re-executes, on detecting a next peak following the previous peak, the maximum value searching operation only in connection with a renewed data block of the delay profile data by the detected peak masking

portion.

13. A CDMA receiver comprising a radio portion for frequency-converting a reception signal into a frequency converted signal, an A/D converter for carrying out analog to digital conversion of the frequency converted signal to produce a digital signal, a multi-path detection circuit for measuring a delay profile of a transmission path from the digital signal to detect timing of a multi-path as multi-path timing, a rake finger portion for receiving the digital signal at the multi-path timing to produce reception data, and a rake combiner for combining the reception data, wherein:

the multi-path detection circuit comprises:

means for dividing delay profile data representative of the delay profile into a plurality of data blocks;

a delay profile memory for storing the respective data blocks;

searching means for searching a maximum value at every one of the data blocks in connection with the delay profile data to determine a peak at every data block as a result of the search; and

generating means for generating the timing of the multi-path with reference to the peak.

14. A multi-path detection circuit as claimed in claim 13, further comprising:

means for renewing the delay profile data into renewed delay profile data by masking a neighboring time region of the delay profile data adjacent to the peak detected so as to detect a next following peak in the renewed delay profile data after the peak;

means for selecting a specific one of the data blocks that includes the peak previously detected; and

control means for making the search means search a following maximum value again only about the specific block of the renewed

delay profile data.

15. A multi-path detection circuit as claimed in claim 14, wherein the control means comprises:

means for judging whether or not the previously detected peak is located on a right-hand side of a center of the specific data block, to produce a result of judgment; and

means for making the searching means re-execute the search in connection with either one of the data blocks adjacent to the specific data block on its right-hand side or left-hand side with reference to the result of judgment.

16. A multi-path detection circuit as claimed in claim 15, wherein the control means comprises:

means for comparing each peak detected with a predetermined reference correlation level to detect a low peak lower than the predetermined reference correlation level; and

means for stopping the search when the low peak is detected.